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This is the ARM
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**ARM7TDMI Technical
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17 April 2001 A First
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Rev 4. 19 September
2001 B Maintenance
update to correct
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errors. 26 November
2004 C Maintenance
update to correct
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DB14-000058-02 ARM

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IEEE Std. 1149.1-

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time a word or phrase

is defined in this

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3.5. Address timing

The ARM7TDMI processor address bus can operate in one of two configurations: pipelined depipelined. Note ARM Limited strongly recommends that pipelined address timing is used in new

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design to obtain optimum system performance. ARM Limited strongly recommends that ALE is tied HI

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